

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in the present application. Claim 1 is amended, Claims 5-7 are withdrawn, and Claims 8-12 are added by the present amendment.

In the outstanding Office Action, Claims 5-7 were withdrawn from consideration; Claims 1-3 were rejected under 35 U.S.C. § 102(b) as anticipated by Hill et al. (U.S. Patent No. 5,220,218, herein "Hill"); and Claim 4 was indicated as allowable if rewritten in independent form.

Applicants thank the Examiner for the indication of allowable subject matter and for the courtesy of an interview extended to Applicants' representative on October 4, 2004. During the interview, differences between the present invention and the applied art were discussed. Further, clarifying claim amendments were also discussed. No agreement was reached, pending the Examiner's detailed consideration of a filed response.

First, a new abstract consistent with amended Claim 1 is presented. No new matter is added.

In response to the rejection of Claims 1-3 under 35 U.S.C. § 102(b) as anticipated by Hill, Claim 1 has been amended to clarify the structure of the claimed semiconductor device. The claim amendments find support in Figure 9. No new matter is added.

Briefly recapitulating, amended Claim 1 is directed to a semiconductor device including plural CMOS transistors with first and second transistors sharing a common first gate electrode and third and fourth transistors sharing a second common gate electrode that is adjacent and parallel to the first gate electrode. The first and third transistors share a common n-type channel MOS region and the second and fourth transistors share a common

p-type channel MOS region. The semiconductor device also includes a wire that connects the common n-type channel MOS region and the common p-type channel MOS region.

In a non-limiting example, Figures 9 and 10 show the common first and second gate electrodes 3, the common n-type channel MOS region 1, the common p-type channel MOS region 2, and the wire 8.

Turning to the applied art, Hill shows in Figure 1 a semiconductor device having two transistors having different gate electrodes and different channel regions. Thus, Hill does not teach or suggest plural CMOS transistors with (i) first and second transistors sharing a common first gate electrode, (ii) third and fourth transistors sharing a common second gate electrode that is adjacent and parallel to the first gate electrode, (iii) the first and third transistors sharing a common n-type channel MOS region, and (iv) the second and fourth transistors sharing a common p-type channel MOS region, as required by amended independent Claim 1.

Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom patentably distinguish over Hill.

New Claims 8-12 have been added to set forth the invention in a varying scope and Applicants respectfully submit the new claims are supported by the originally filed specification (see for example Figures 9-13). No new matter has been added.

New independent Claim 8 is directed to a semiconductor device that includes, inter alia, a first insulating film formed on a first gate electrode, a second insulating film formed on a second gate electrode, a third insulating film formed on a side surface of the first electrode and a side surface of the first insulating film, a fourth insulating film formed on a side surface of the second gate electrode and a side surface of the second insulating film, an interlayer insulating film formed over and between the first and second gate electrodes, and having an opening exposing the third and fourth insulating films and the first and second insulating

films located between the first and said second electrodes, and a buried wiring formed in the opening and not extending over the interlayer insulating film. New Claim 11 recites similar features as Claim 8.

Hill, which has been discussed above, does not teach or suggest four insulating layers and an interlayer insulating layer having an opening in which a wiring is formed such that the wiring does not extend over the interlayer insulating film, as required by new Claim 8.

Accordingly, it is respectfully submitted that independent Claims 8 and 11 and each of the claims depending therefrom patentably distinguish over Hill.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

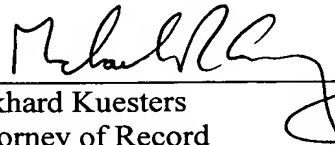
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